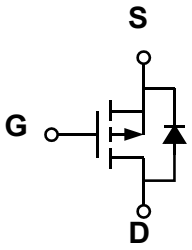
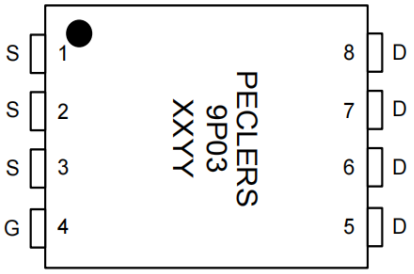
30V P-Channel Enhancement Mode MOSFET

Schematic diagram



Marking and pin assignment

PDFN3×3-8L
（Top View）



Description

The PECN9P03QR uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in load switch and battery protection applications.

General Features

- V_{DS} =-30V，I_D =-9.0A
  $R_{DS(ON)}$(Typ.)=23.2mΩ @V_{GS}=-4.5V
  $R_{DS(ON)}$(Typ.)=18.3mΩ @V_{GS}=-10V
- High power and current handing capability
- Lead free product is acquired
- Surface mount package

Application

- Battery protection
- Load switch

Package

- PDFN3×3-8L

Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
PECN9P03QR	-55°C to +150°C	PDFN3×3-8L	5000

Absolute Maximum Ratings (TA=25℃ unless otherwise noted)

parameter	symbol	limit	unit
Drain-source voltage	V_{DS}	-30	V
Gate-source voltage	V_{GS}	±20	V
Drain current-continuous[a]@Tj=125℃	I_D	-9.0	A
-pulse *d*[b]	I_{DM}	-40	A
Drain-source Diode forward current	Is	-2.5	A
Maximum power dissipation	P_D	35	W
Operating junction Temperature range	Tj	-55—150	℃

Electrical Characteristics (TA=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF Characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-30	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=-30V, V_{GS}=0V	-	-	-1	μA
Gate-body leakage	I_{GSS}	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
ON Characteristics						
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1.00	-1.6	-3.0	V
Drain-source on-state resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=4.5A	-	18.3	22	mΩ
		V_{GS}=4.5V, I_D=4.5A		23.2	34	
Forward transconductance	gfs	V_{GS}=-5V, I_D=-9A	-	24	-	S
Dynamic Characteristics						
Input capacitance	C_{ISS}	V_{DS}=-15V ,V_{GS}=0V f=1.0MHz	-	1040	1250	pF
Output capacitance	C_{OSS}		-	180	-	
Reverse transfer capacitance	C_{RSS}		-	125	175	
Switching Characteristics						
Turn-on delay time	$t_{D(ON)}$	V_{DS}=-15V R_L=2.2 Ω V_{GS}=-10V R_{GEN}=3 Ω	-	10	-	ns
Rise time	tr		-	5.5	-	
Turn-off delay time	$t_{D(OFF)}$		-	26	-	
Fall time	tf		-	9	-	
Total gate charge	Qg(10V)	V_{DS}=-15V,I_D=-9A V_{GS}=-10V	-	19	-	nC
Total gate charge	Qg(4.5V)			9.6		
Gate-source charge	Qgs		-	3.6	-	
Gate-drain charge	Qgd		-	4.6	-	
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode forward voltage	V_{SD}	V_{GS}=0V,Is=-1.0A	-	-0.75	-1.0	V

Notes:

a. The value of Rth JA is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C. The value in any given application depends on the user's specific boarddesign.

b. The power dissipation P_D is based on $T_{J(MAX)}$=150℃, using ≤ 10s junction-to-ambient thermal resistance.

c. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

d. The Rth JA is the sum of the thermal impedence from junction to lead Rth JL and lead to ambient.

e. The static characteristics in Figures 1 to 6 are obtained using <300us pulses, duty cycle 0.5% max.

f. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of TJ(MAX)=150°C. The SOA curve provides a single pulse rating.

Thermal Characteristics

Thermal Resistance junction-to ambient	Rth JA	3.57	℃/W

Typical Performance Characteristics

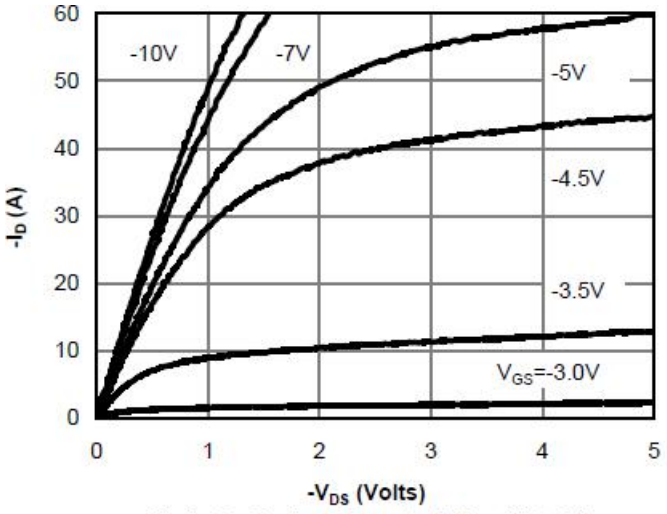


Fig 1: On-Region Characteristics (Note E)

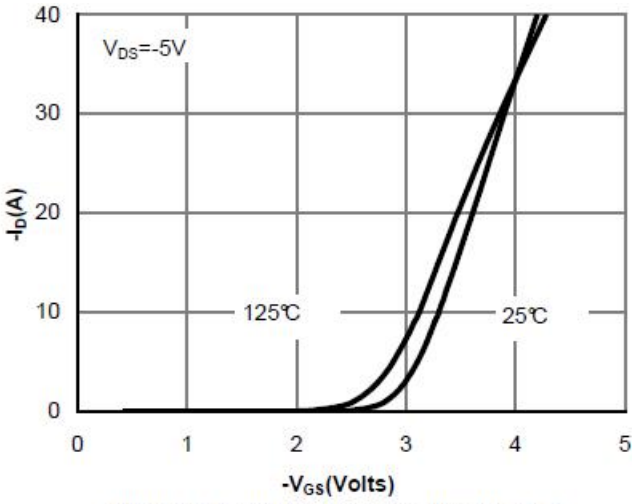


Figure 2: Transfer Characteristics (Note E)

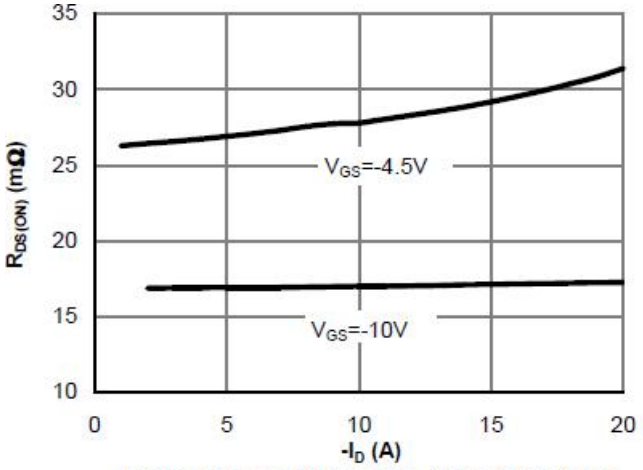


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

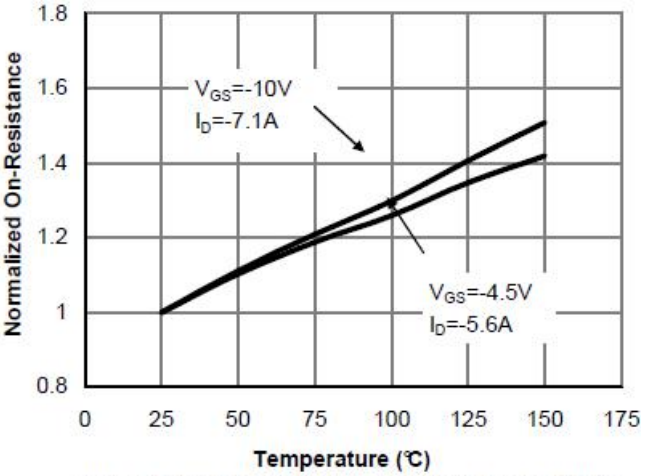


Figure 4: On-Resistance vs. Junction Temperature (Note E)

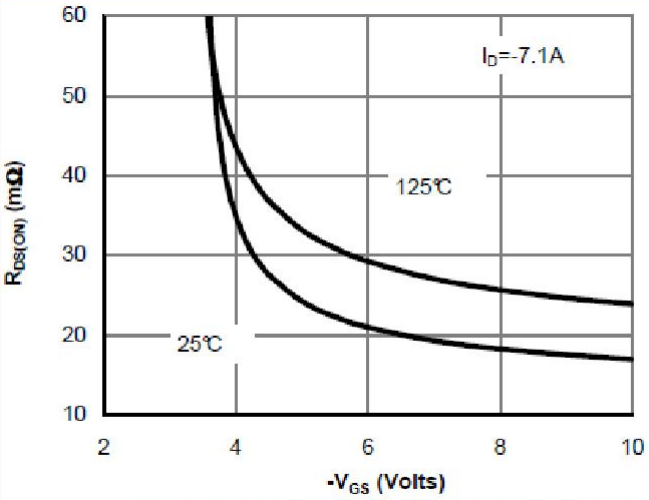


Figure 5: On-Resistance vs. Gate-Source Voltage

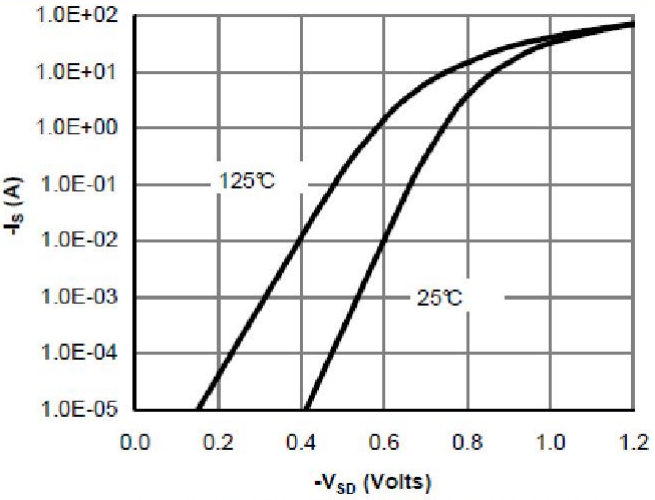


Figure 6: Body-Diode Characteristics (Note E)

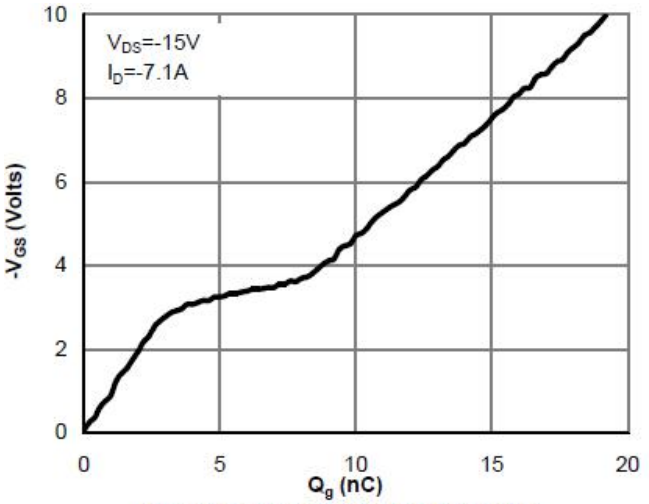


Figure 7: Gate-Charge Characteristics

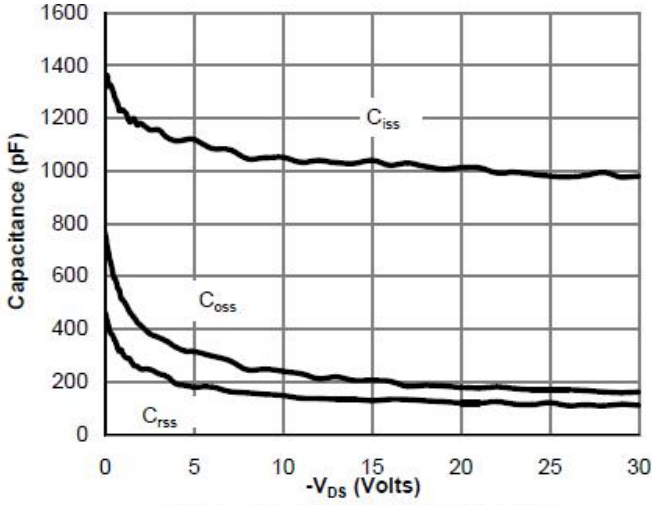


Figure 8: Capacitance Characteristics

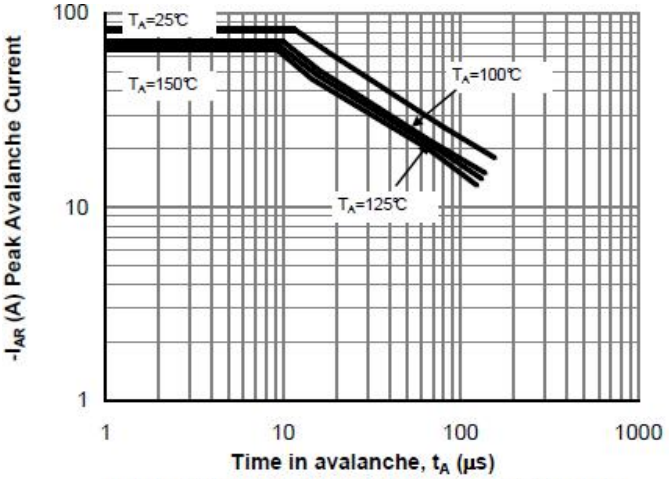


Figure 9: Single Pulse Avalanche capability (Note C)

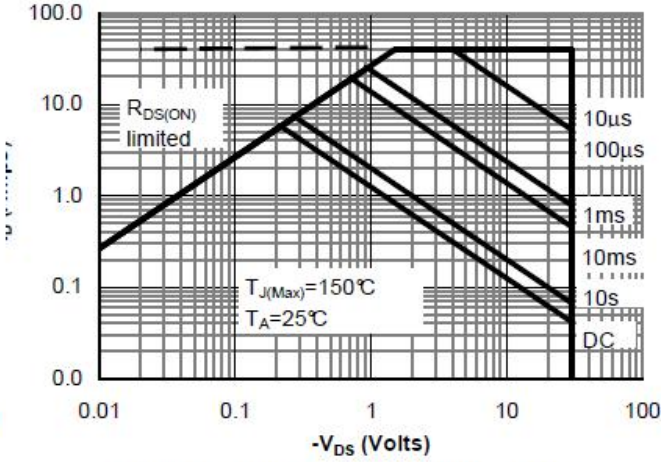


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

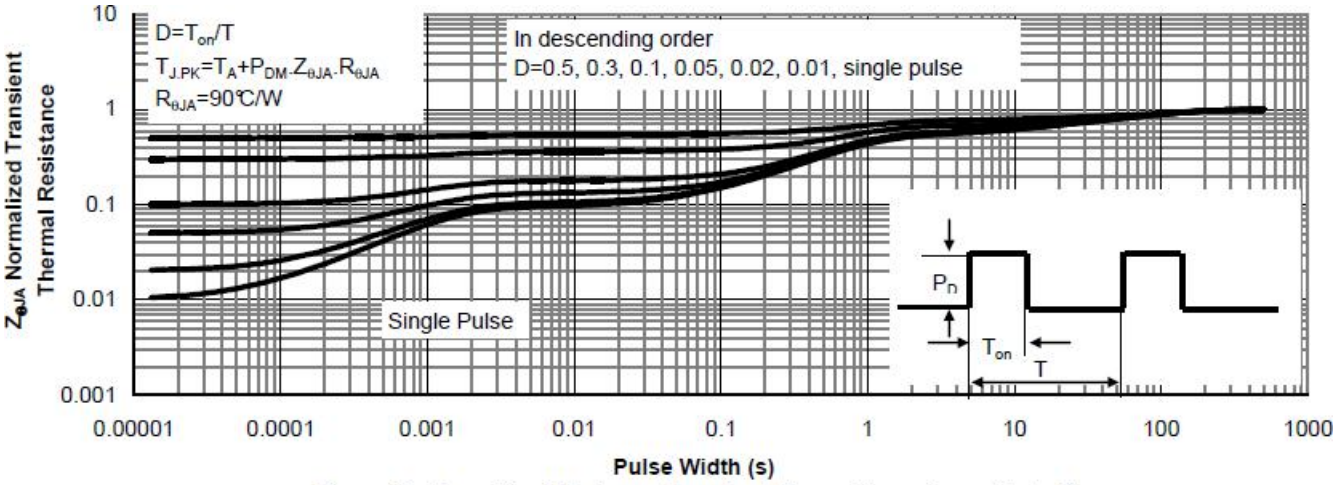
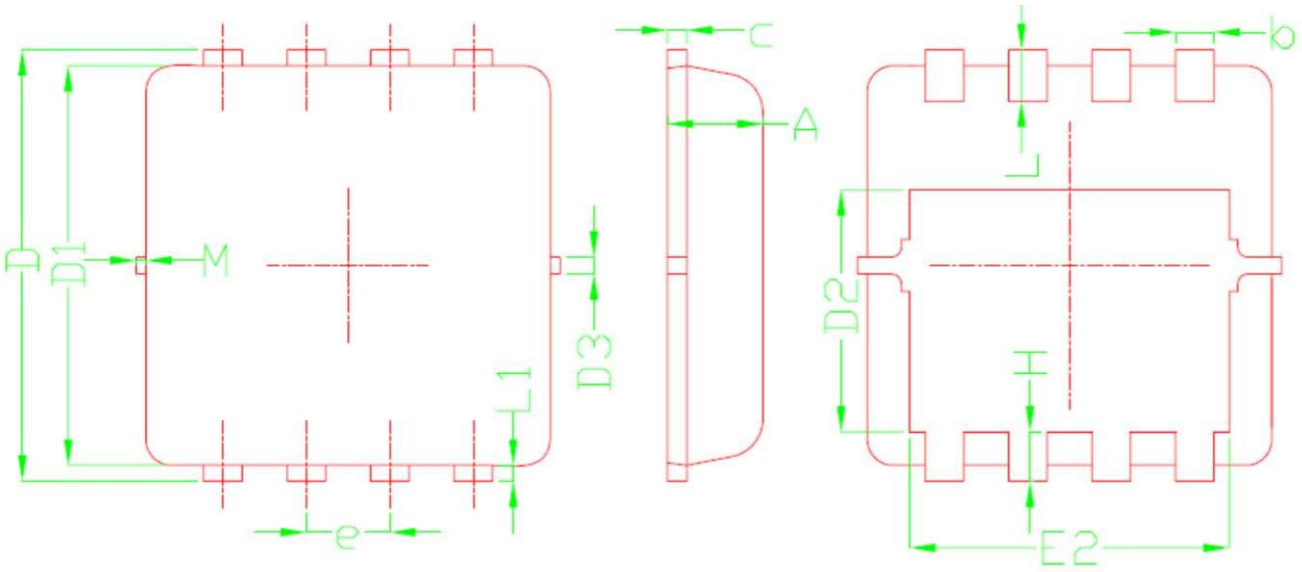
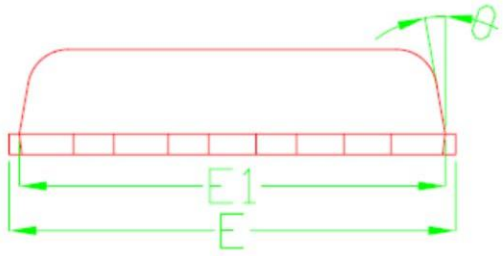


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

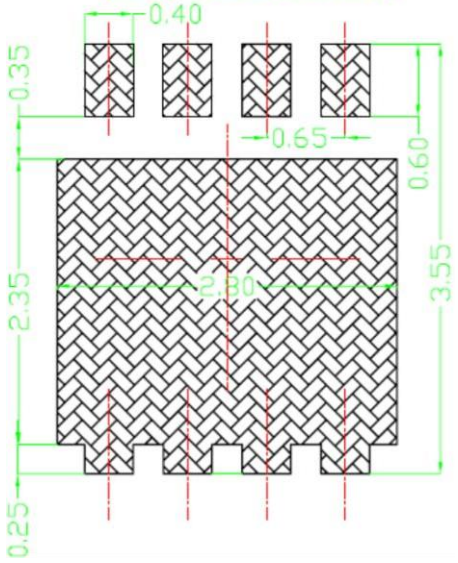
Package Information

- PDFN3×3-8L





Land Pattern
(Only for Reference)



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
θ	---	10°	12°
M	*	*	0.15
* Not specified			