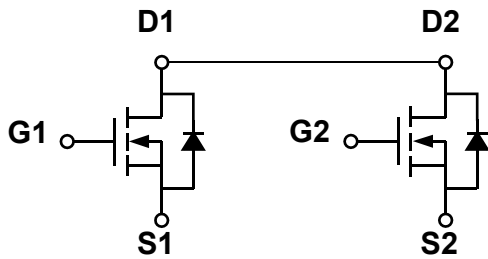
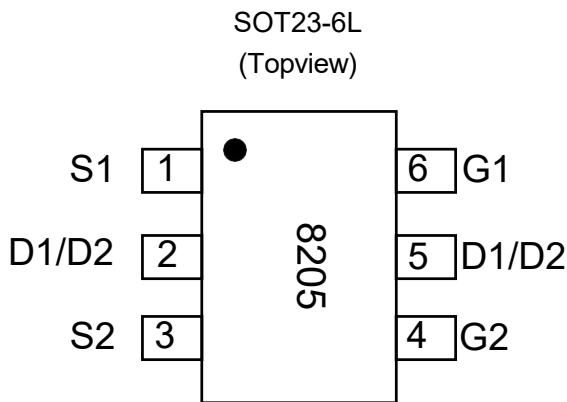


20V Dual N-Channel Enhancement Mode MOSFET

Schematic diagram



Marking and pin assignment



Description

The PECN8205MR uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

- ◆ $V_{DS} = 20V, I_D = 6.5A$
 $R_{DS(ON)} = 14.6m\Omega$ (typical) @ $V_{GS} = 4.5V$
 $R_{DS(ON)} = 18.4m\Omega$ (typical) @ $V_{GS} = 2.5V$
- ◆ High power and current handling capability
- ◆ Lead free product is acquired
- ◆ Surface mount package

Application

- ◆ Battery protection
- ◆ Load switch
- ◆ Power management

Package

- ◆ SOT23-6L



Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
PECN8205MR	-55°C to +150°C	SOT-23	3000

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter	symbol	limit	unit	
Drain-source voltage	V_{DS}	20	V	
Gate-source voltage	V_{GS}	±12	V	
Drain Current-Continuous (Silicon Limited)	I_D	$T_A = 25^\circ C$	6.5	A
		$T_A = 75^\circ C$	4	
Pulsed Drain Current (Package Limited)	I_{DM}	25	A	
Maximum power dissipation	P_D	$T_A = 25^\circ C$	1.5	W
		$T_A = 75^\circ C$	1	
Operating junction Temperature range	T_j	-55—150	°C	

Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF Characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
Gate-body leakage	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$	-	-	± 100	nA
ON Characteristics						
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.7	1.2	V
Drain-source on-state resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=6A$	-	14.6	22	m Ω
		$V_{GS}=2.5V, I_D=5.5A$	-	18.4	27	
Forward transconductance	gfs	$V_{DS}=5V, I_D=6A$	-	10	-	S
Dynamic Characteristics						
Input capacitance	C_{ISS}	$V_{DS}=10V, V_{GS}=0V$ $f=1.0MHz$	-	900	-	pF
Output capacitance	C_{OSS}		-	215	-	
Reverse transfer capacitance	C_{RSS}		-	105	-	
Switching Characteristics						
Turn-on delay time	$t_{D(ON)}$	$V_{DS}=10V$ $V_{GS}=4.5V$ $I_D=6A$ $R_{GEN}=6\Omega$	-	10	-	ns
Rise time	tr		-	11	-	
Turn-off delay time	$t_{D(OFF)}$		-	34	-	
Fall time	tf		-	29	-	
Total gate charge	Qg	$V_{DS}=10V, I_D=6A$ $V_{GS}=4.5V$	-	12	-	nC
Gate-source charge	Qgs		-	2.4	-	
Gate-drain charge	Qgd		-	1	-	

Thermal Characteristics

Thermal Resistance junction-to ambient	Rth JA	100	°C/W
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Typical Performance Characteristics

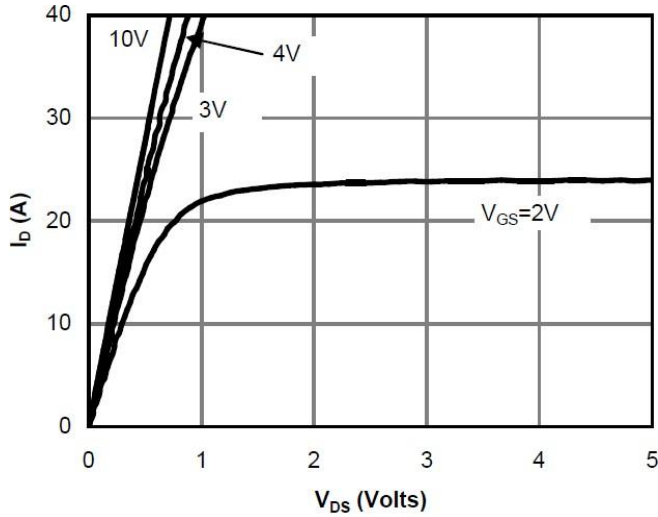


Figure 1: On-Region Characteristics (Note E)

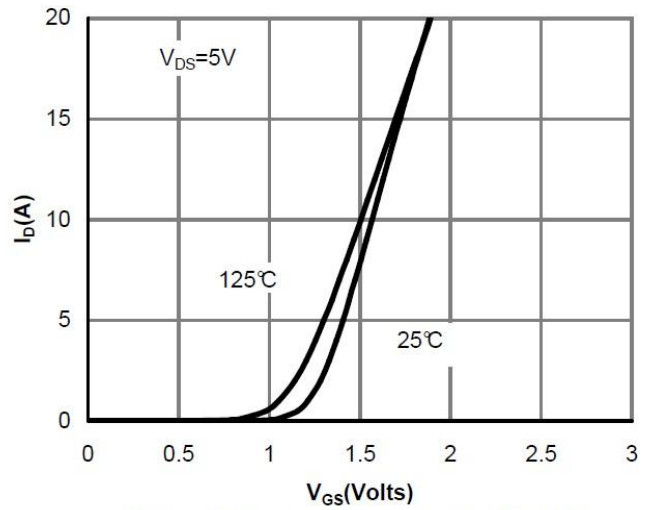


Figure 2: Transfer Characteristics (Note E)

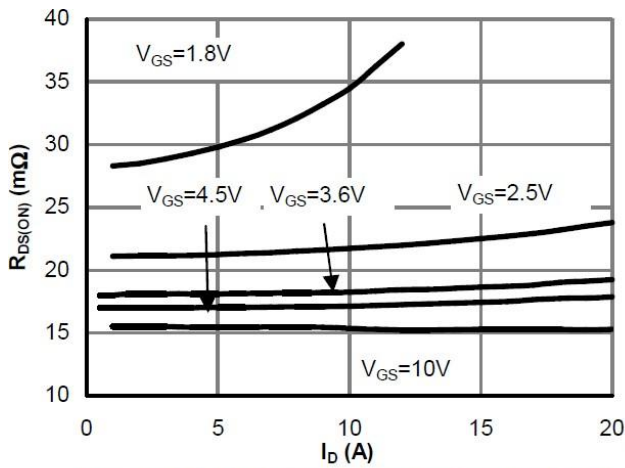


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

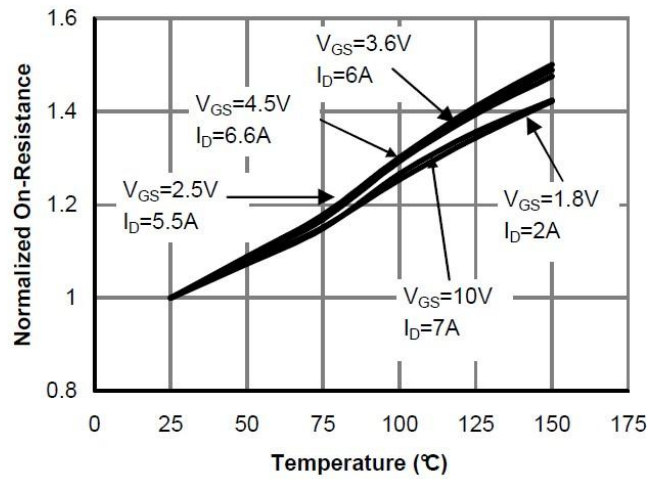


Figure 4: On-Resistance vs. Junction Temperature (Note E)

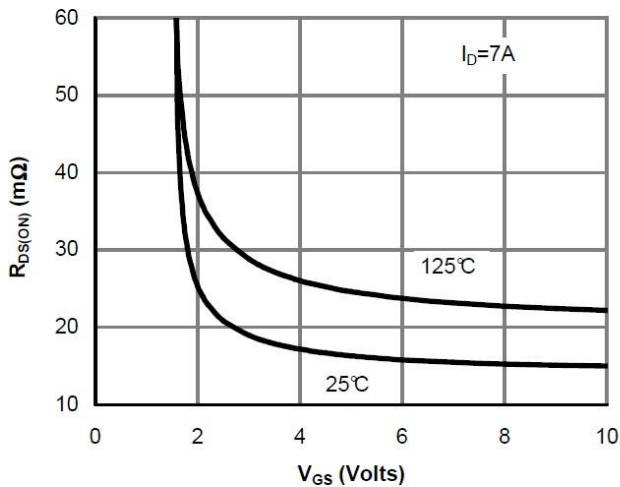


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

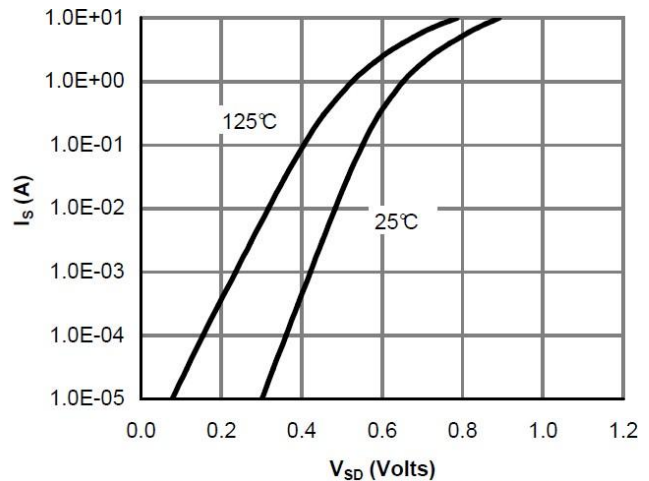


Figure 6: Body-Diode Characteristics (Note E)

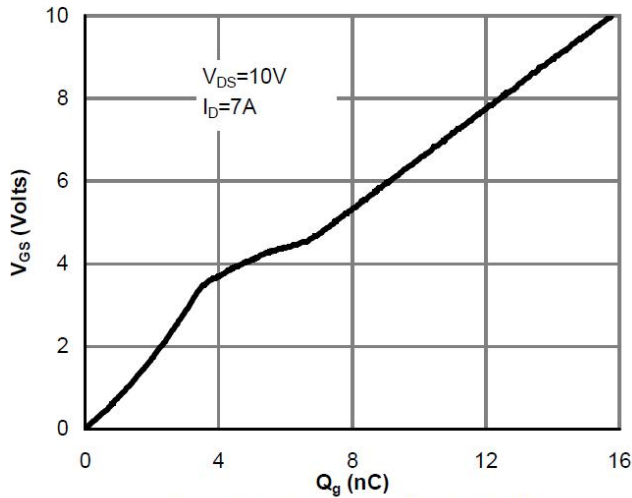


Figure 7: Gate-Charge Characteristics

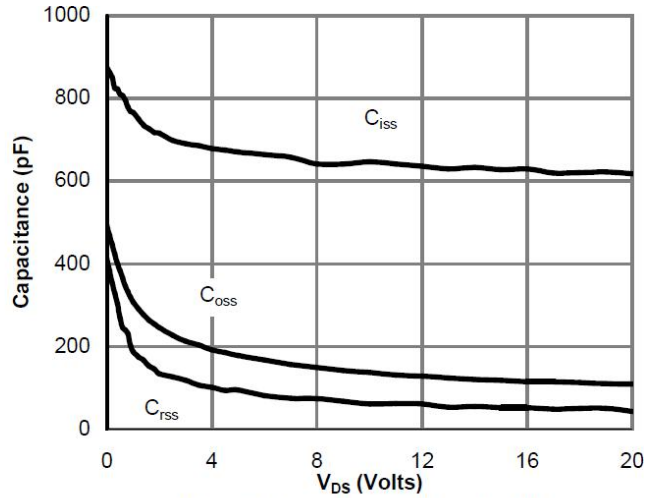


Figure 8: Capacitance Characteristics

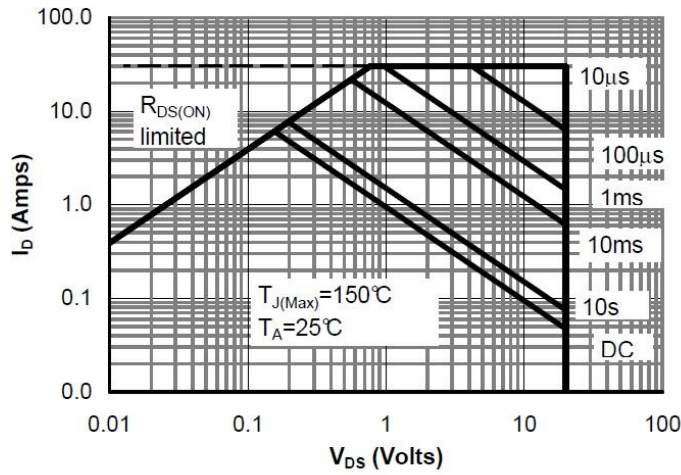


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

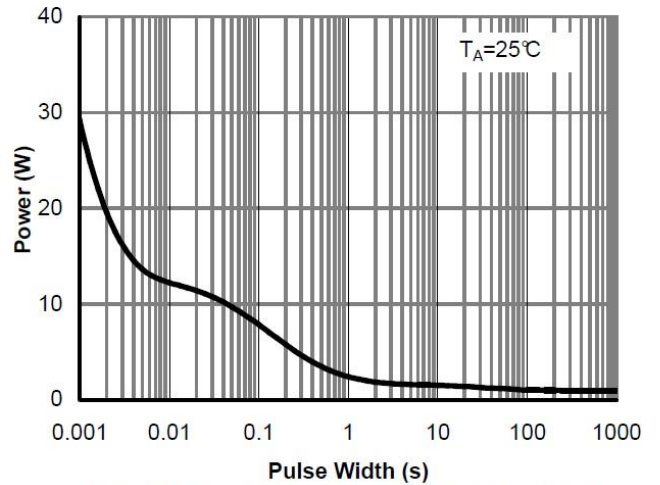


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

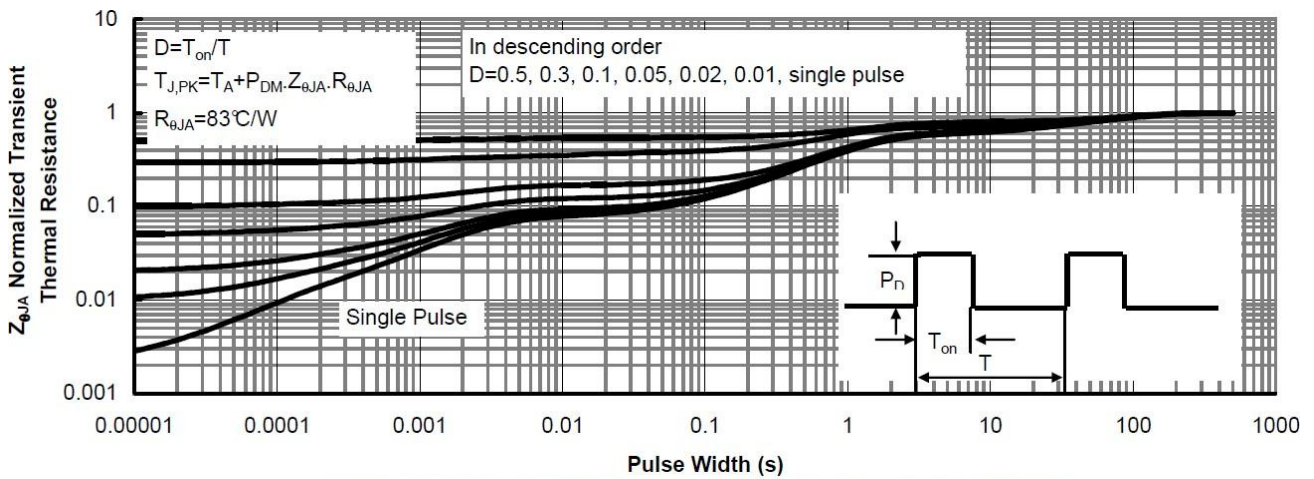
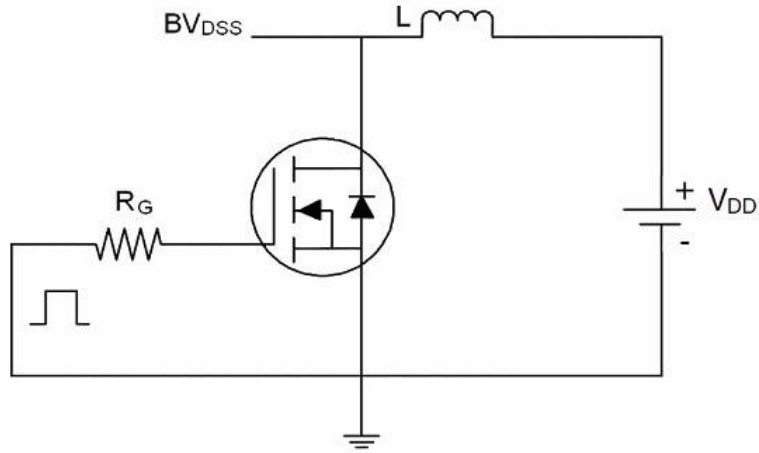


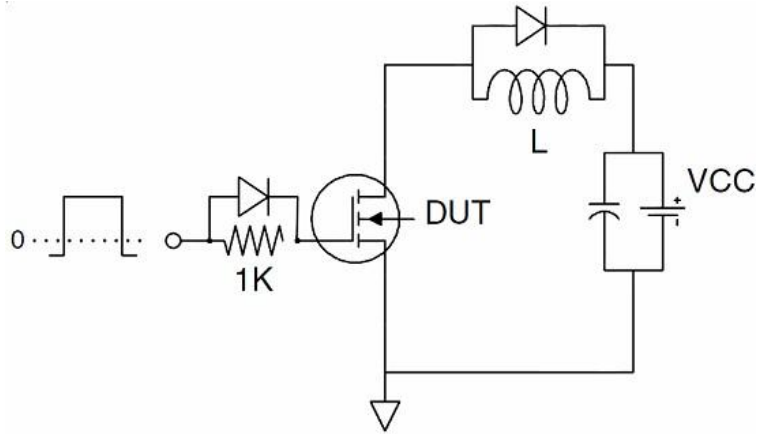
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Test Circuit:

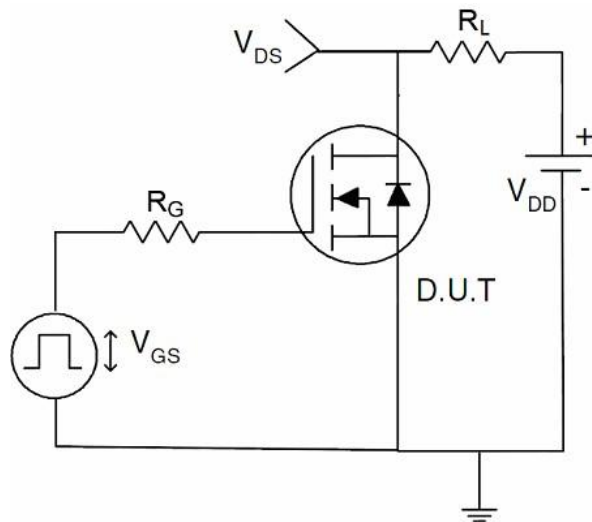
1 、 EAS Test Circuit



2 、 Gate Charge Test Circuit

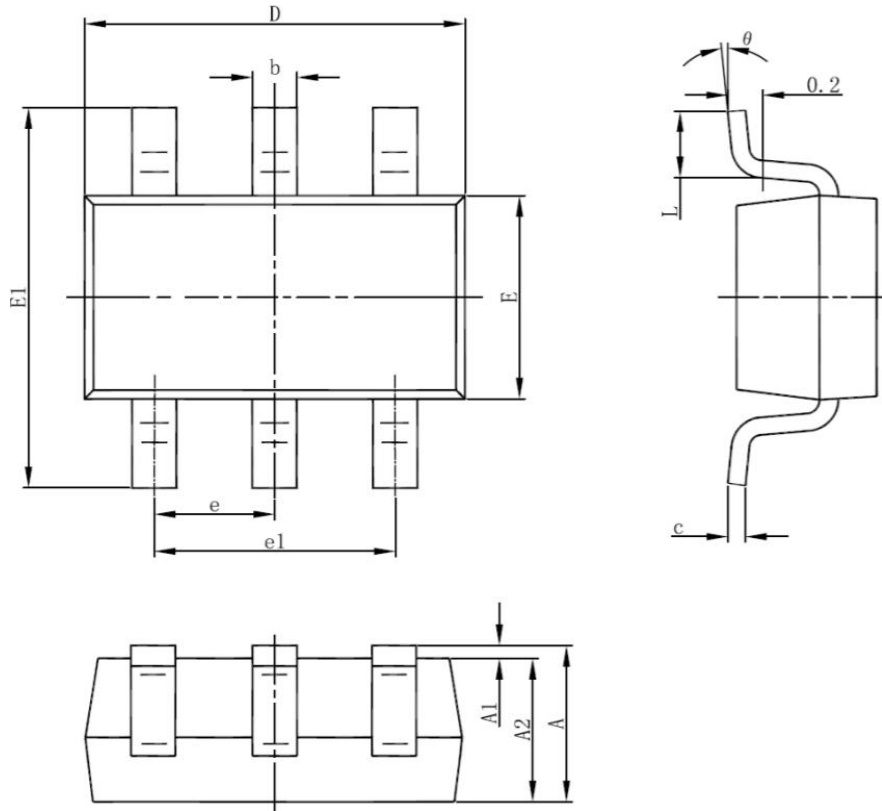


3 、 Switch Time Test Circuit



Package Information

- SOT23-6L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°