

30V N-Channel MOS**Description**

The PECN20N03QR uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. Standard Product NP20N03 is Pb-free (meets ROHS & Sony 259 specifications).

General Features

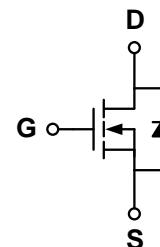
- ◆ $V_{DS} = 30V$ $I_D = 10A$
 $R_{DS(ON)}(\text{Typ.}) = 9m\Omega$ @ $V_{GS} = 10V$
 $R_{DS(ON)}(\text{Typ.}) = 14.5m\Omega$ @ $V_{GS} = 4.5V$
- ◆ Lead free product is acquired
- ◆ Surface mount package

Application

- ◆ High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- ◆ Networking DC-DC Power System
- ◆ Load switch

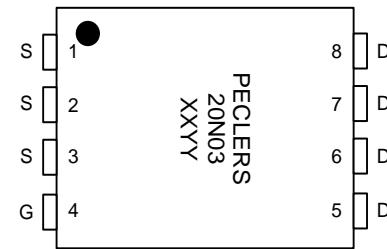
Package

- ◆ PDFN3×3-8L

Schematic diagram**Marking and pin assignment**

PDFN3×3-8L

(Top View)

**Ordering Information**

Part Number	Storage Temperature	Package	Devices Per Reel
PECN20N03QR	-55°C to +150°C	PDFN3×3-8L	3000

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter	symbol	limit	unit
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	20	A
		14	
Pulsed Drain Current	I_{DP}	80	A
Avalanche Current	I_{AS}	17	A
Avalanche energy(L=0.1mH)	E_{AS}	14	mJ
Maximum power dissipation	P_D	15	W
Power Dissipation – Derate above 25°C		1.67	
Operating junction Temperature range	T_j	-55—150	°C

Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	30	-	-	V
BVDSS Temperature Coefficient	△BV _{DSS} /△T _J	Reference to 25°C, ID=1mA		33		mV/°C
Zero gate voltage drain current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
		T _J =85°C	-	-	30	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V	-	-	±100	nA
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.6	2.5	V
Drain-source on-state resistance ¹	R _{DS(ON)}	V _{GS} =10V, I _D =10A	-	9	12	mΩ
		V _{GS} =4.5V, I _D =10A		14.5	16	
On Status Drain Current	I _{D(ON)}	V _{DS} =10V, V _{GS} =10V	20	-	-	A
Diode Characteristics						
Diode Forward Voltage ¹	V _{SD}	I _{SD} =1A, V _{GS} =0V	-	0.8	1.1	V
Diode Continuous Forward Current	I _S		-	-	18	A
Reverse Recovery Time	t _{rr}	I _F =20A, dI/dt=100A/us	-	9	-	ns
Reverse Recovery Charge	Q _{rr}		-	15	-	nC
Dynamic Characteristics²						
Gate Resistance	R _G	V _{GS} =0V, V _{DS} =0V, f=1MHz	-	3	-	Ω
Input capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =20V f=1.0MHz	-	595	-	pF
Output capacitance	C _{OSS}		-	98	-	
Reverse transfer capacitance	C _{RSS}		-	70	-	
Turn-on delay time	t _{D(ON)}	V _{GS} =10V, V _{DD} =15V, R _L =20Ω, I _D =10A, R _G =3.3Ω	-	4.6	-	ns
Turn-on Rise time	t _r		-	12.2	-	
Turn-off delay time	t _{D(OFF)}		-	26.6	-	
Turn-off Fall time	t _f		-	8	-	
Total gate charge	Q _g	V _{GS} =4.5V, I _D =10A V _{DS} =15V	-	13.6		nC
Gate-source charge	Q _{gs}			1.6		
Gate-drain charge	Q _{gd}		-	3.6	-	
Drain-Source Diode Characteristics						
Diode forward voltage	V _{SD}	I _{SD} =50A, V _{GS} =0V	-	0.8	1.1	V

Note: 1: Pulse test; pulse width ≤ 300ns, duty cycle ≤ 2%.

2: Guaranteed by design, not subject to production testing.

Thermal Characteristics

Parameter	Symbol	Typical	Unit
Thermal Resistance-Junction to Case	R _{θjc}	1.7	°C/W
Thermal Resistance junction-to ambient	R _{θja}	62.5	

Typical Performance Characteristics

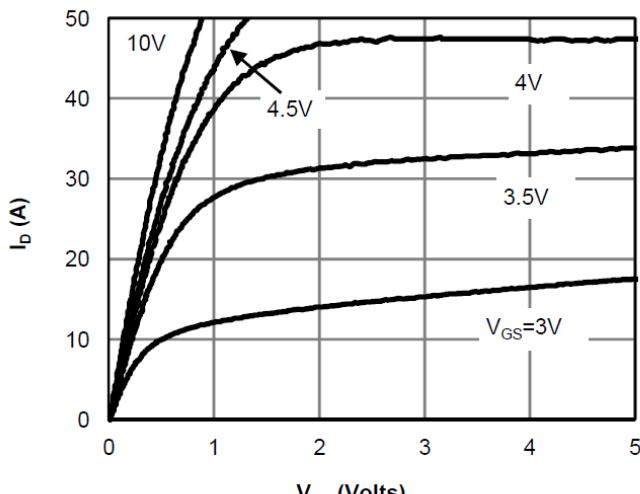


Fig 1: On-Region Characteristics (Note E)

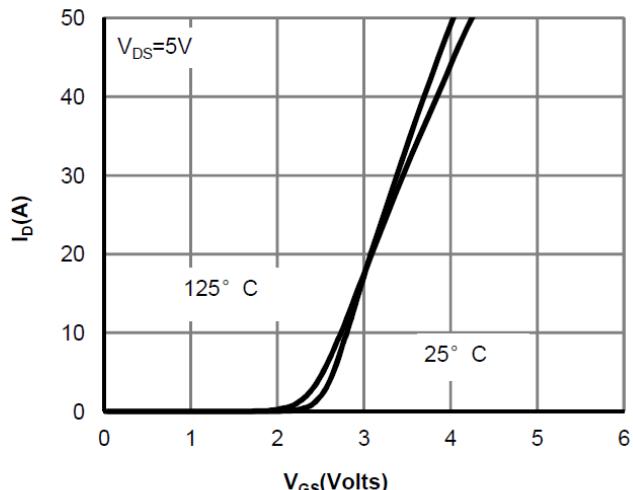


Figure 2: Transfer Characteristics (Note E)

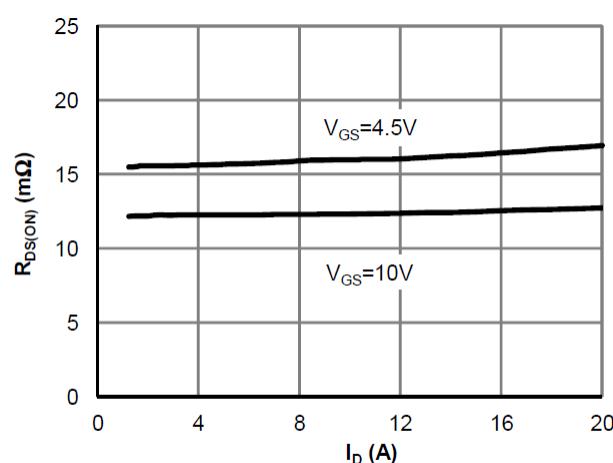


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

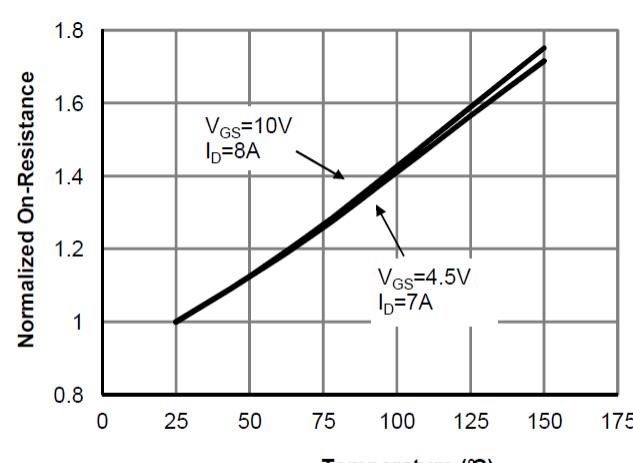


Figure 4: On-Resistance vs. Junction Temperature (Note E)

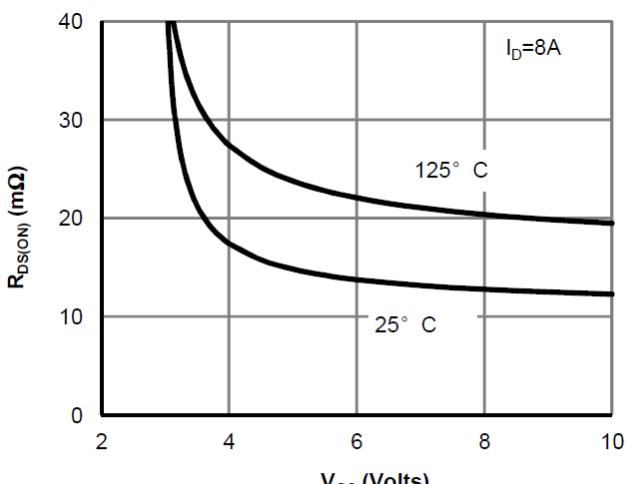


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

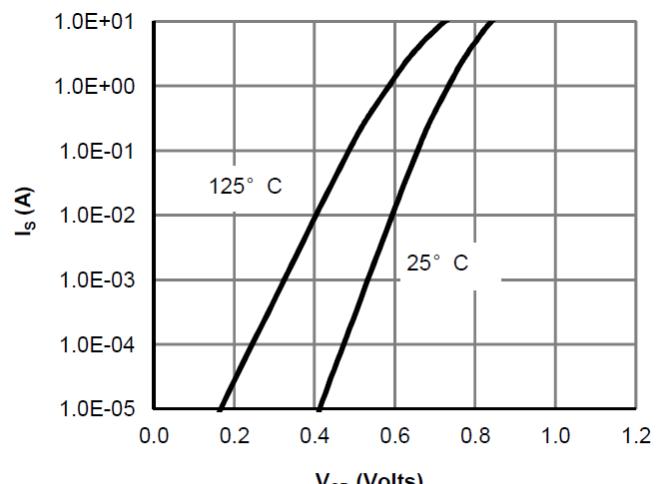
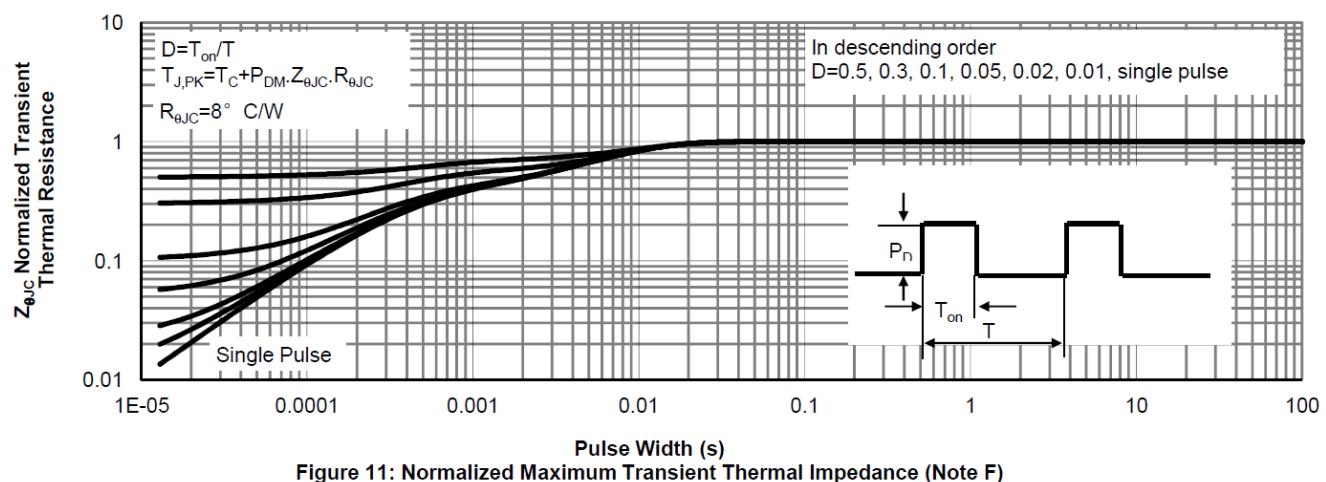
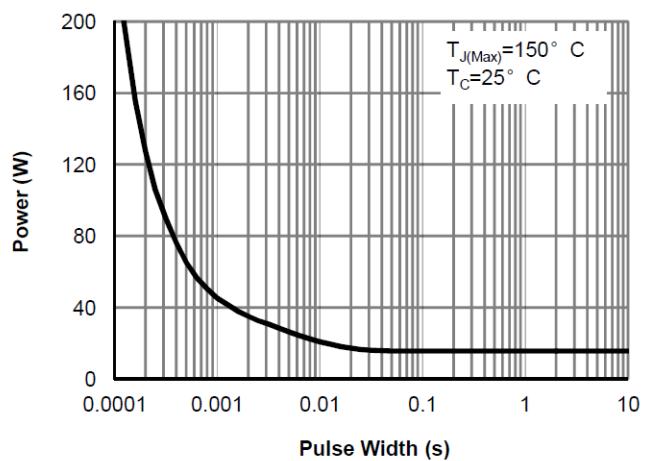
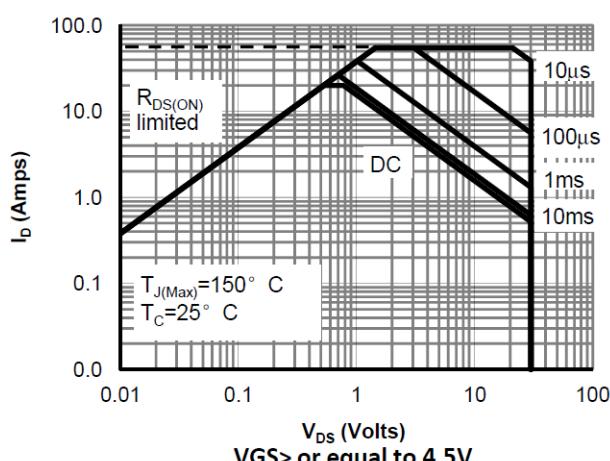
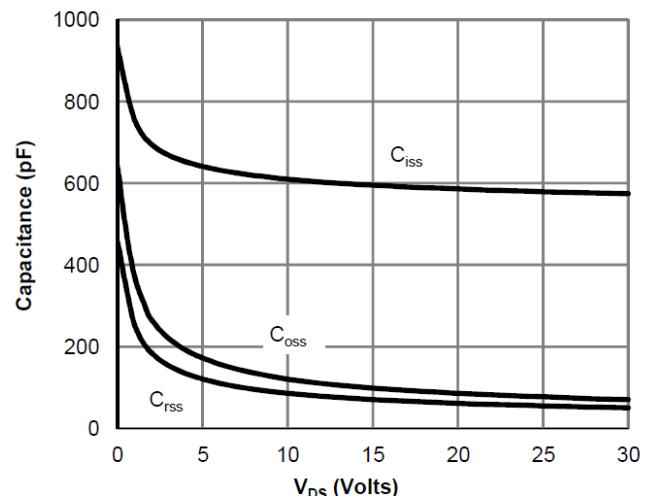
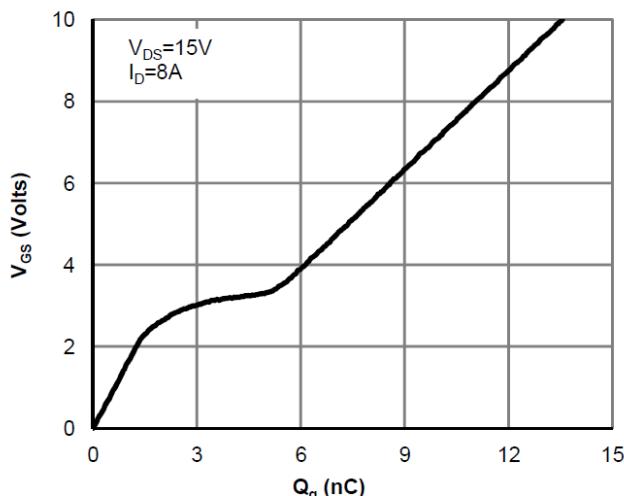


Figure 6: Body-Diode Characteristics (Note E)



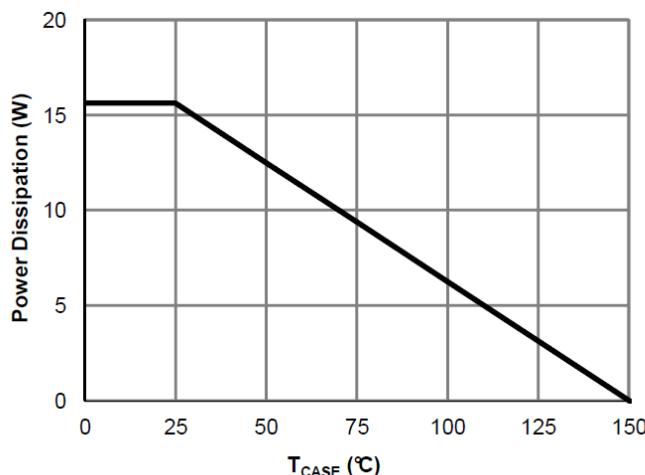


Figure 12: Power De-rating (Note F)

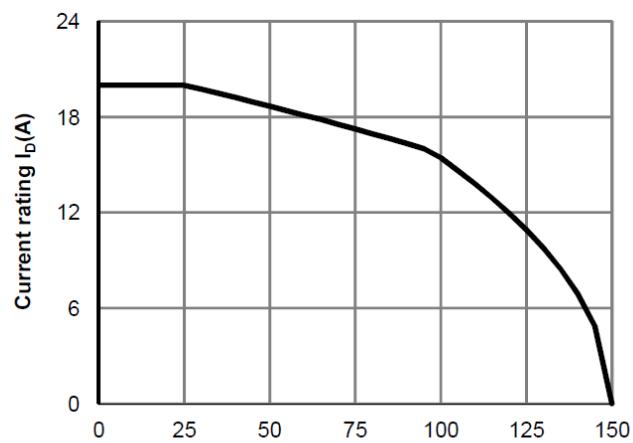


Figure 13: Current De-rating (Note F)

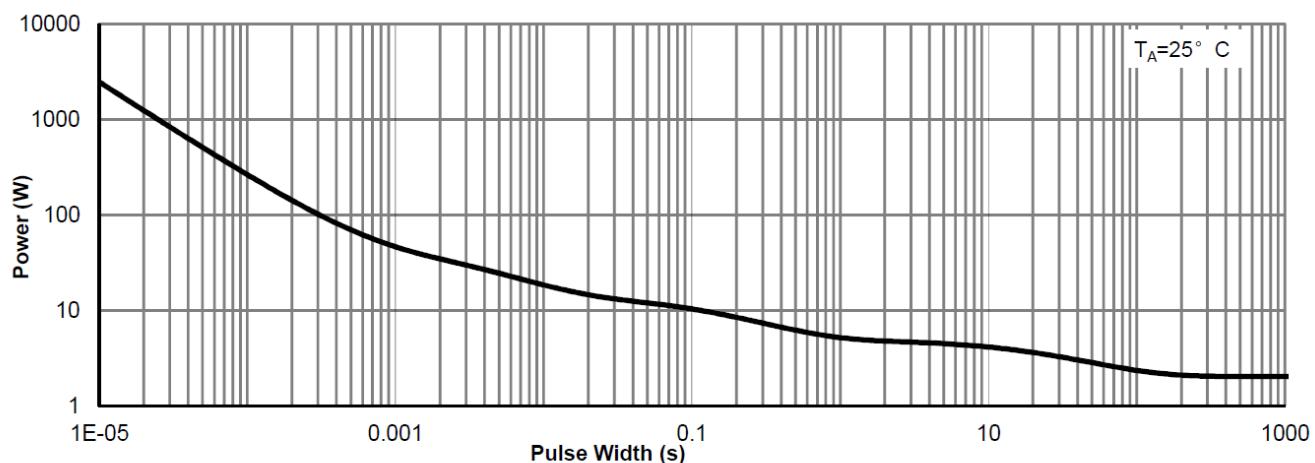


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

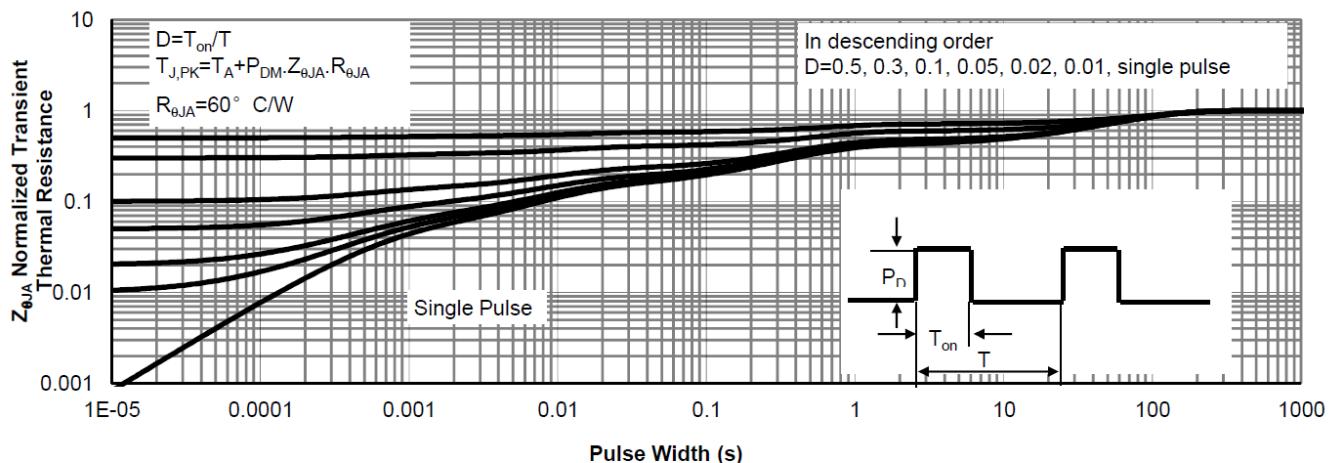
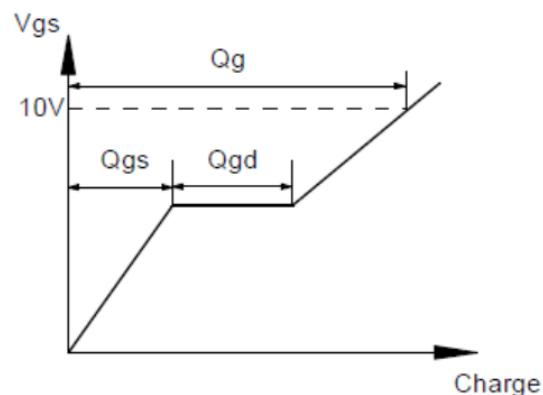
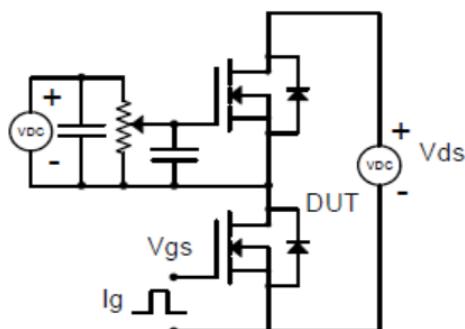
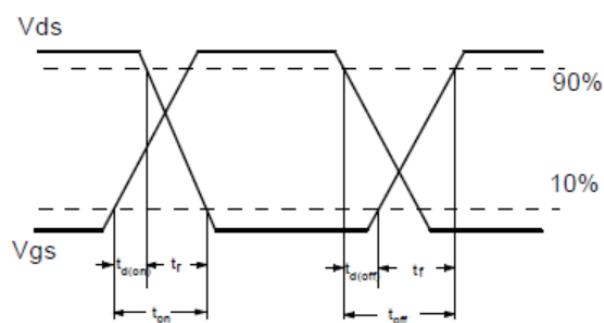
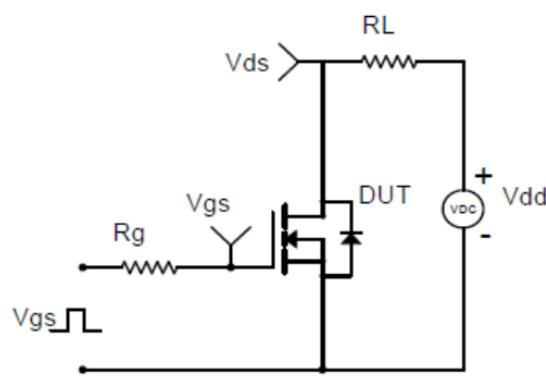


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

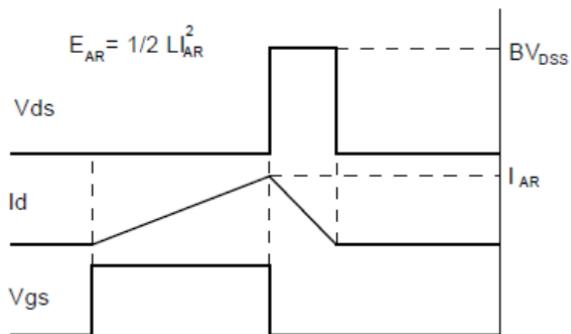
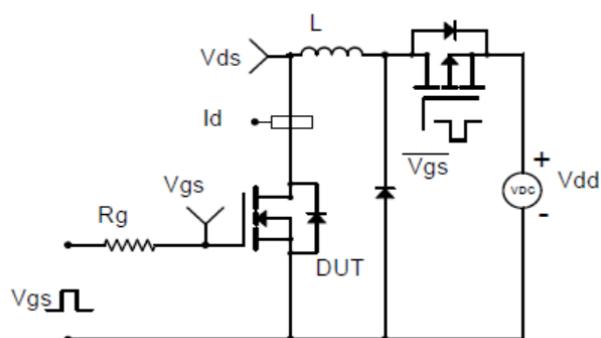
Gate Charge Test Circuit & Waveform



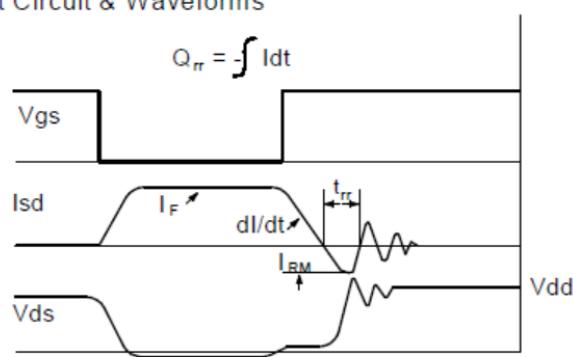
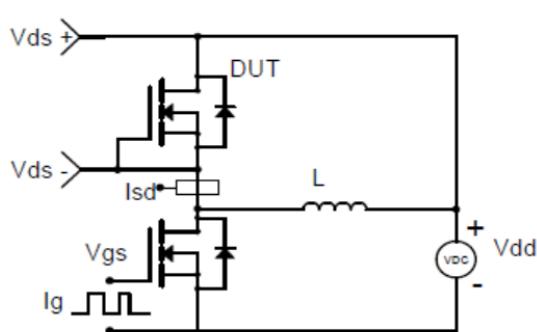
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Information

- PDFN3×3-8L

